1. A circuit for converting an input current to an output voltage, comprising:

a load impedance across which the output voltage is generated;

a common gate FET serving as a current buffer stage, including a source coupled to an input current node, a gate, and a drain coupled to a DC reference voltage through the load impedance;

a diode-connected FET serving as a floating current reference, including a source coupled to the input node and the source of the common gate FET, a gate and a drain coupled to the gate of the common gate FET;

a DC current source coupled to the source of the diode-connected FET capable of setting a common gate FET drain current;

a capacitance coupled between a DC reference voltage and the coupled gates of the common gate FET and diode-connected FET; and

a DC current path from the input node to a DC reference voltage.

2. The circuit of claim 1, wherein said load impedance comprises a resistor.

3. The circuit of claim 1, wherein the DC current path includes a resistor.

4. The circuit of claim 1, wherein a relative size ratio of the FETs is selected to minimize excess bias current from the floating current diode-connected FET while avoiding substantial degradation of current transfer of the common gate FET.

5. The circuit of claim 1, wherein at least one of the FETs is of a type selected from the group consisting of NMOS transistors, PMOS transistors, MESFETs, JFETs, and HEMTs.

6. An optical receiver, comprising:

a photodetector for converting an optical signal into a current signal;

a circuit coupled to the photodetector at an input node for converting the current signal to an output voltage, including a load impedance across which the output voltage is generated, a common gate stage FET serving as a current buffer, including a source coupled to the input node and a drain coupled to a DC reference voltage through the load impedance, a diode-connected FET serving as a floating current reference, including a source coupled to the input node and the source of the common gate stage FET, and a gate and a drain coupled to the gate of the common gate stage FET, a DC current source coupled to the source of the diode-connected FET setting a common gate stage FET drain current, a capacitance coupled between a DC reference voltage and the coupled gates of the common gate stage FET and diode-connected FET, and a DC current path from the input node to a DC reference voltage.

7. The optical receiver of claim 6, wherein said load impedance comprises a resistor.

8. The optical receiver of claim 7, wherein the DC current path includes a resistor.

9. The optical receiver of claim 6, wherein a relative size ratio of the FETs is selected to minimize excess bias current from the floating current diode-connected FET while avoiding substantial degradation of current transfer of the common gate FET.

10. The optical receiver of claim 6, wherein at least one of the FETs is of a type selected from the group consisting of NMOS transistors, PMOS transistors, MESFETs, JFETs, and HEMTs.

11. A circuit for converting an input current to an output voltage, comprising:

a load impedance across which the output voltage is generated;

a common base bipolar transistor serving as a current buffer stage, including a emitter coupled to the input node, a base, and a collector coupled to a DC reference voltage through the load impedance;

a diode-connected bipolar transistor serving as a floating current reference, including a emitter coupled to the input node and the emitter of the common base bipolar transistor, and a base and a collector coupled to the base of the common base bipolar transistor;

a DC current source coupled to the collector of the diode connected bipolar transistor setting a common base bipolar transistor collector current;

a capacitance coupled between a DC reference voltage and the coupled bases of the common base bipolar transistor and diode-connected bipolar transistor; and

a DC current path from the input node to a DC reference voltage.

12. The circuit of claim 11, wherein said load impedance comprises a resistor.

13. The circuit of claim 11, wherein the DC current path includes a resistor.

14. The circuit of claim 11, wherein a relative size ratio of the bipolar transistors is selected to minimize excess bias current from the floating current diode-connected bipolar transistor while avoiding substantial degradation of current transfer of the common base bipolar transistor.

15. The circuit of claim 11, wherein at least one of the bipolar transistors is of a type selected from the group consisting of NPN bipolar junction transistors, PNP bipolar junction transistors, NPN heterojunction bipolar transistors, and PNP heterojunction bipolar transistors.

16. An optical receiver, comprising:

a photodetector for converting an optical signal into a current signal;

a circuit coupled to the photodetector at an input node for converting the current signal to an output voltage, including a load impedance across which the output voltage is generated, a common base bipolar transistor serving as a current buffer stage, including an emitter coupled to the input node, a base, and a collector coupled to a DC reference voltage through the load impedance, a diode-connected bipolar transistor serving as a floating current reference, including an emitter coupled to the input node and the emitter of the common base bipolar transistor, and a base and a collector coupled to the base of the common base bipolar transistor, a DC current source coupled to the collector of the diode connected bipolar transistor setting a common base bipolar transistor collector current, a capacitance coupled between a DC reference voltage and the coupled bases of the common base bipolar transistor and diode-connected bipolar transistor, and a DC current path from the input node to a DC reference voltage.

17. The optical receiver of claim 16, wherein said load impedance comprises a resistor.

18. The optical receiver of claim 16, wherein the DC current path includes a resistor.

19. The optical receiver of claim 16, wherein a relative size ratio of the bipolar transistors is selected to minimize excess bias current from the floating current diode-connected bipolar transistor while avoiding substantial degradation of current transfer of the common base bipolar transistor.

20. The optical receiver of claim 16, wherein at least one of the bipolar transistors is of a type selected from the group consisting of NPN bipolar junction transistors, PNP bipolar junction transistors, NPN heterojunction bipolar transistors, and PNP heterojunction bipolar transistors.